



PATENT  
Atty. Dkt. AMAT/8830/FEP/PCVD/PJS

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:  
Ma, et al.

Serial No.: 10/784,904

Confirmation No.: 6141

Filed: February 23, 2004

For: Gate Electrode Dopant Activation Method For Semiconductor Manufacturing

MAIL STOP AMENDMENT  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Group Art Unit: 2812  
Examiner: William M. Brewster

**CERTIFICATE OF MAILING**

37 CFR 1.8

I hereby certify that this correspondence is being deposited on July 22, 2005 with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

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Dear Sir:

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The Applicants, and the Attorney who signs below on the basis of the information supplied by the inventor and the information in his file, submit herewith patents, publications, or other information of which they are aware, which may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

While the information submitted in this Supplemental Information Disclosure Statement may be material pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication, or other information referred to therein is prior art for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97, this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possibly material information as defined under 37 CFR § 1.56(a) exists.

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The patents and/or publications submitted herewith are set forth on the attached Form PTO-1449.

Applicants certify that all references submitted with this disclosure were cited in a communication from a foreign patent office dated June 23, 2005, which communication is enclosed, not more than three months prior to the filing of this Supplemental Information Disclosure Statement.

If the sum of \$180.00 is due under 37 CFR § 1.17(p) pursuant to § 1.97, the Commissioner is hereby authorized to charge this fee, and any other fee necessary to make this submission timely, to the Deposit Account No. 20-0782/AMAT/8830/KMT.

Respectfully submitted,

  
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Application Number	10/784,904
Filing Date	February 23, 2004
First Named Inventor	Ma, et al.
Group Art Unit	2812
Examiner Name	William M. Brewster
Attorney Docket Number	AMAT/8830/FEP/PCVD/PJS

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**SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT BY  
APPLICANT**

(Use as many sheets as necessary)

Sheet

1

of

1

Submission Date

July 22, 2005

### U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
	A1	US-6100171	08/08/2000	Ishida	
	A2	US-5966605	10/12/1999	Ishida	
	A3	US-5399506	03/21/1995	Tsukamoto	
	A4				
	A5				
	A6				
	A7				
	A8				
	A9				
	A10				
	A11				

### FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)				
	B1	WO 01/71787 A1	09/27/2001	Varian Semiconductor Equipment Associates, Inc.		
	B2					
	B3					
	B4					

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
	C1	International Search Report dated June 23, 2005 regarding International Application No. PCT/US2005/004318 (AMAT/8830-PCT)	
	C2	Goto, et al. "Ultra-Low Contact Resistance for Deca-nm MOSFETs by Laser Annealing", Electron Devices Meeting, 1999. IEDM Technical Digest. International Washington, DC, USA 5-8 Dec. 1999, Piscataway, NJ, USA, IEEE, US, 5 December 1999 (1999-12-02), pp. 931-933, XP010372206	

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